WHAT IS CLAIMED IS:

1. A module having first and second primary surfaces and having a first end, the module comprising:

a first set of input finger connectors disposed on at least one of the first and second primary surfaces proximate to the first end;

a first set of output finger connectors disposed on at least one of the first and second primary surfaces proximate to the first end;

a second set of input finger connectors disposed on at least one of the first and second primary surfaces proximate to the first end;

a second set of output finger connectors disposed on at least one of the first and second primary surfaces proximate to the first end; and

a bus including a first channel extending from the first set of input finger connectors to the first set of output finger connectors and a second channel extending from the second set of input finger connectors to the second set of output finger connectors.

2. The module of claim 1 further comprising

at least one first integrated circuit (IC) populating at least one of the first and second primary surfaces, the first channel connected to the at least one first IC; and

at least one second IC populating at least one of the first and second primary surfaces, the second channel connected to the at least one second IC.

3. The module of claim 2, wherein the first IC and the second IC are memory devices.

4. The module of claim 2, wherein the at least one first IC is a plurality of first ICs and the at least one second IC is a plurality of second ICs.

5. The module of claim 4 wherein the first channel and the second channel allow simultaneous independent access to at least some of the first and second ICs.

6. The module of claim 2 further comprising:

a third set of input finger connectors disposed on at least one of the first and second primary surfaces;

a third set of output finger connectors disposed on at least one of the first and second primary surfaces;

a fourth set of input finger connectors disposed on at least one of the first and second primary surfaces; and

a fourth set of output finger connectors disposed on at least one of the first and second primary surfaces, wherein the bus further includes:

a third channel extending from the third set of input finger connectors to the third set of output finger connectors; and

a fourth channel extending from the fourth set of input finger connectors to the fourth set of output finger connectors.

7. The module of claim 6, further comprising:

at least one third IC populating at least one of the first and second primary surfaces, the third channel connected to the at least one third IC; and

at least one fourth IC populating at least one of the first and second primary surfaces, the fourth channel connected to the at least one fourth IC.

8. The module of claim 7 wherein the first channel, the second channel, the third channel, and the fourth channel each allow simultaneous independent access to the respective ICs.

9. The module of claim 6 wherein the first set of input finger connectors, the first set of output finger connectors, the second set of input finger connectors, and the second set of output finger connectors are disposed on the first primary surface, and the third set of input finger connectors, the third set of output finger connectors, the fourth set of input finger connectors, and the fourth set of output finger connectors are disposed on the second primary surface.

10. The module of claim 2 wherein

the at least one first IC is a plurality of first ICs;

the first channel has a first characteristic impedance and is coupled to a plurality of paths, each of the paths is coupled to one of the first ICs, and

the plurality of paths has a combined effective impedance substantially equal to the first characteristic impedance.

11. The module of claim 6, wherein the first set of input finger connectors, the first set of output finger connectors, the second set of input finger connectors, and the second set of output finger connectors are disposed on the first primary surface and the third set of input finger connectors, the third set of output finger connectors, the fourth set of input finger connectors, and the fourth set of output finger connectors are disposed on the second primary surface.

12. A bus system comprising:

a motherboard including motherboard connectors and bus segments electrically coupling the motherboard connectors; and

a plurality of modules arranged from a first module to a last module, wherein each of the plurality of modules includes a bus having a first channel and a second channel, the first channel connecting a first set of input finger connectors proximate to a first end to a first set of output finger connectors proximate to the first end and the second channel connecting a second set of input finger connectors proximate to the first end to a second set of output finger connectors proximate to the first end, the bus electrically coupled to one of the motherboard connectors, wherein each of the modules is mechanically coupled to one of the motherboard connectors.

13. The bus system of claim 12, wherein each of the modules further comprises at least one first IC connected to the first channel and at least one second IC connected to the second channel.

14. The bus system of claim 13 wherein the bus segments of the motherboard electrically connect the first set of output finger connectors of the first module to the first set of input finger connectors of a second module of the plurality of modules and the second set of output finger connectors of the first module to the second set of input finger connectors of the second module.

15. The bus system of claim 14 wherein the bus segments of the motherboard electrically connect the first set of output finger connectors of the last module to a first bus termination and the second set of output finger connectors of the last module to a second bus termination.

16. The bus system of claim 13 wherein, within each of the modules, the first channel and the second channel allow simultaneous independent access to the at least one first IC and the at least one second IC.

17. A module comprising:

a first printed circuit board having first and second primary surfaces and having a first end and a second end;

at least one first integrated circuit (IC) populating at least one of the first and second primary surfaces;

a set of finger connectors disposed on the first printed circuit board proximate to the first end;

a first bus segment disposed on the first printed circuit board and coupled to the set of finger connectors and the at least one first IC;

a conductive interconnect having a second bus segment, the conductive interconnect connected to the first printed circuit board proximate to the second end and adapted to mechanically connect to a second printed circuit board, the second bus segment electrically coupled to the first bus segment and capable of being electrically coupled to a third bus segment disposed on the second printed circuit board; and

a bus comprising at least the first and second bus segments.

18. The module of claim 17 further comprising the second printed circuit board having the third bus segment disposed thereon, wherein the conductive interconnect is mechanically connected to the second printed circuit board and the third bus segment is electrically coupled to the second bus segment.

19. The module of claim 18 further comprising a connector electrically and mechanically connecting the conductive interconnect to the second printed circuit board.

20. The module of claim 19, wherein the conductive interconnect has a first edge and a second edge opposite the first edge, the first printed circuit board being connected to the conductive interconnect at the first edge, the connector being connected to the conductive interconnect at the second edge.

21. The module of claim 20, further comprising at least one second IC disposed on the second printed circuit board.

22. The module of claim 21, wherein the at least one second IC is coupled to the third bus segment.

23. The module of claim 22 wherein the third bus segment is terminated with a first bus termination.

24. The module of claim 22 wherein the bus further comprises the third bus segments.

25. The module of claim 24, wherein the bus includes a first channel and a second channel, the first channel terminated with the first bus termination and the second channel terminated with a second bus termination.

26. The module of claim 21 wherein the bus substantially traverses the first printed circuit board between the first and second ends.

27. The module of claim 21 wherein the bus comprises a first channel and a second channel and the set of finger connectors comprises a first set of finger connectors and a second set of finger connectors, the first channel coupled to the first set of finger connectors and the second channel coupled to the second set of finger connectors, the first channel and the second channel allowing simultaneous independent access to the at least one first IC and the at least one second IC.

28. The module of claim 19 wherein the second printed circuit board is removably engaged with the connector.

29. The module of claim 18 further comprising a spacer adapted to maintain the first and second printed circuit boards in substantially parallel, spaced apart relation to one another.

30. The module of claim 29, wherein the spacer is attached to one of the first and second primary surfaces of the first printed circuit board proximate to the second end.

31. The module of claim 19 wherein the connector is oriented to maintain the second printed circuit board substantially parallel to at least one of the first and second primary surfaces of the first printed circuit board.

32. The module of claim 17 wherein the conductive interconnect is flexible.

33. The module of claim 32, wherein the conductive interconnect is a flex circuit.

34. The module of claim 21, wherein the at least first IC is a plurality of first ICs and the at least one second IC is a plurality of second ICs.

35. The module of claim 34, wherein each of the first and second ICs are memory devices.

36. A bus system comprising:

a motherboard including a motherboard connector and a first bus segment electrically coupled to the motherboard connector; and

a module comprising:

a first printed circuit board having first and second primary surfaces and having a first end and a second end;

a set of finger connectors disposed on the first printed circuit board proximate to the first end, the finger connectors electrically connected to the motherboard connector;

at least one first integrated circuit (IC) disposed on the first printed circuit board;

a second bus segment disposed on the first printed circuit board and coupled to the set of finger connectors and the at least one first IC; and

a conductive interconnect having a third bus segment, the conductive interconnect connected to the first printed circuit board proximate to the second end and adapted to mechanically connect to a second printed circuit board, the third bus segment electrically coupled to the second bus segment and capable of being electrically coupled to a fourth bus segment disposed on the second printed circuit board.

37. The bus system of claim 36, wherein the module is mechanically connected to the motherboard connector.

38. The bus system of claim 37, wherein the module further comprises the second printed circuit board having the fourth bus segment disposed thereon, wherein the conductive interconnect is mechanically connected to the second printed circuit board and the fourth bus segment is electrically coupled to the third bus segment.

39. The bus system of claim 38, further comprising a connector electrically and mechanically connecting the conductive interconnect to the second printed circuit board.

40. The bus system of claim 38, wherein the module further comprises at least one second IC disposed on the second printed circuit board and coupled to the fourth bus segment.

41. The bus system of claim 40, wherein the second printed circuit board is removably engaged with the connector.

42. The bus system of claim 38, wherein the fourth bus segment is terminated with a first bus termination.

43. The bus system of claim 38, wherein the first, second, third and fourth bus segments form a bus.

44. The bus system of claim 43, wherein the bus includes a first channel and a second channel, the first channel terminated with the first bus termination and the second channel terminated with a second bus termination.

45. The bus system of claim 44, wherein the first and second channel allow simultaneous independent access to the at least one first IC and the at least one second IC.

46. The bus system of claim 36, wherein conductive interconnect is flexible.

47. The bus system of claim 36, wherein the at least first IC is a plurality of first ICs and the at least one second IC is a plurality of second ICs.

48. The module of claim 47, wherein each of the first and second ICs are memory devices.

49. The bus system of claim 38, wherein the second printed circuit board has a set of printed circuit board finger connectors, wherein the set of printed circuit board finger connectors and the set of finger connectors are adapted to alternatively engage the motherboard connector.

50. A module having first and second primary surfaces and having a first end, the module comprising:

a plurality of integrated circuits (ICs) populating at least one of the first and second primary surfaces;

a first set of input finger connectors disposed on at least one of the first and second primary surfaces;

a second set of input finger connectors disposed on at least one of the first and second primary surfaces;

a first terminator disposed on at least one of the first and second primary surfaces;

a second terminator disposed on at least one of the first and second primary surfaces;

a first bus including a first channel extending from the first set of input finger connectors to the first terminator, the first bus connected to a first IC of the plurality of ICs; and

a second bus including a second channel extending from the second IC of input finger connectors to the second terminator, the second bus connected to a second IC of the plurality of ICs.

51. The module of claim 50 wherein the first set of input finger connectors and the second set of input finger connectors are disposed proximate to the first end.

52. The module of claim 50 wherein the first IC of the plurality of ICs and the second IC of the plurality of ICs are mutually exclusive.

53. The module of claim 50 wherein the first channel and the second channel allow simultaneous independent access to the plurality of ICs.

54. The module of claim 50 further comprising:

a third set of input finger connectors disposed on at least one of the first and second primary surfaces;

a fourth set of input finger connectors disposed on at least one of the first and second primary surfaces;

a third terminator disposed on at least one of the first and second primary surfaces;

a fourth terminator disposed on at least one of the first and second primary surfaces; and

a third bus including a third channel extending from the third set of input finger connectors to the third terminator; and

a fourth bus including a fourth channel extending from the fourth set of input finger connectors to the fourth terminator.

55. The module of claim 54 wherein the third bus is connected to a third IC of the plurality of ICs and wherein the fourth bus is connected to a fourth IC of the plurality of ICs.

56. The module of claim 55 wherein the first IC of the plurality of ICs, the second IC of the plurality of ICs, the third IC of the plurality of ICs, and the fourth IC of the plurality of ICs are mutually exclusive.

57. The module of claim 54 wherein the first set of input finger connectors, the second set of input finger connectors, the third set of input finger connectors, and the fourth set of input finger connectors are disposed proximate to the first end.

58. The module of claim 54 wherein the first set of input finger connectors and the second set of input finger connectors are disposed on the first primary surface, and the third set of input finger connectors and the fourth set of input finger connectors are disposed on the second primary surface.

59. The module of claim 54 wherein the first channel, the second channel, the third channel, and the fourth channel each allow simultaneous independent access to the plurality of ICs.

60. The module of claim 50 wherein the first channel has a first characteristic impedance and is coupled to a plurality of paths, each of the paths being coupled to at least one of the plurality of ICs, and wherein the plurality of paths have a combined effective impedance substantially equal to the first characteristic impedance.

61. The module of claim 50 wherein the first bus is connected to a first set of the plurality of ICs, the first set comprising the first IC, and the second bus is connected to a second set of the plurality of ICs, the second set comprising the second IC.

62. The module of claim 61, wherein each of the ICs are memory devices.

63. A bus system comprising:

a motherboard including motherboard connectors and bus segments electrically coupling the motherboard connectors;

a first module including a first ingress connector, a first egress connector, a first integrated circuit (IC), and a first channel, the first channel coupled to the first ingress connector, the first egress connector, and the first IC;

a second module including a second ingress connector, a second egress connector, a second IC, and a second channel, the second channel coupled to the second ingress connector, the second egress connector, and the second IC; and

a termination module including a first channel terminator and a second channel terminator, the first channel terminator coupled to the first channel of the first module through a first set of the motherboard connectors and the second channel terminator coupled to the second channel of the second module through a second set of the motherboard connectors.

64. The bus system of claim 63, wherein the first and second ICs are memory devices.

65. The bus system of claim 64 wherein the first channel and the second channel allow simultaneous independent access to the first memory device and the second memory device.

66. The bus system of claim 63 wherein the termination module further includes a third IC coupled to the first channel.

67. The bus system of claim 66, wherein the third IC is a memory device.

68. The bus system of claim 63 wherein the bus segments of the motherboard electrically connect the first egress connector to the first channel terminator and the second egress connector to the second channel terminator.

69. A bus system comprising:

a motherboard including motherboard connectors and bus segments electrically coupling the motherboard connectors, the motherboard connectors including a first ingress connector for a first module slot, a first egress connector for the first module slot, a second ingress connector for a second module slot, a second egress connector for the second module slot, a third ingress connector for a third module slot, and a fourth ingress connector for the third module slot, and the bus segments including a first bus segment coupled to the first ingress connector, a second bus segment routed so as to occupy a region of the motherboard located between the first ingress connector and the first egress connector and coupled to the second ingress connector.

70. The bus system of claim 69 wherein the bus segments further comprise a third bus segment coupling the first egress connector to the third ingress connector and a fourth bus segment coupling the second egress connector to the fourth ingress connector.

71. The bus system of claim 70 wherein the first bus segment and the third bus segment are electrically connected by a first module connected to the first ingress connector and the first egress connector and the second bus segment and the fourth bus segment are electrically connected by a second module connected to the second ingress connector and the second egress connector.

72. A bus system comprising:

a motherboard including motherboard connectors and bus segments electrically coupling the motherboard connectors;

a first module including a first ingress connector, a first egress connector, a second ingress connector, and a first terminator, wherein the first ingress connector is electrically coupled to the first egress connector and the second ingress connector is electrically coupled to the first terminator;

a second module including a third ingress connector, a second egress connector, a fourth ingress connector, and a second terminator, wherein the third ingress connector is electrically coupled to the second egress connector and the fourth ingress connector is electrically coupled to the second terminator; and wherein the first ingress connector, the first egress connector, the second ingress connector, the second egress connector, the third ingress connector, and the fourth ingress connector are coupled to the motherboard connectors and wherein a first set of the bus segments couple the first egress connector to the fourth ingress connector and a second set of the bus segments couple the second egress connector to the second ingress connector, thereby providing a first channel coupling the first ingress connector, the first egress connector, the fourth ingress connector, and the second terminator and a second channel coupling the third ingress connector, the second egress connector, the second ingress connector, and the first terminator

73. The bus system of claim 72 wherein the first channel is coupled to a first integrated circuit (IC) of the first module and the second channel is coupled to a second IC of the second module, the first channel and the second channel allowing simultaneous independent access to the first IC and the second IC.

74. The bus system of claim 73, wherein the first and second ICs are memory devices.

75. The bus system of claim 74 wherein the first channel is further coupled to a third IC of the second module and the second channel is further coupled to a fourth IC of the first module.

76. The bus system of claim 75, wherein the third and fourth ICs are memory devices.

77. The bus system of claim 72 wherein the first channel is coupled to a first memory device of the second module and the second channel is coupled to a second memory device of the first module, the first channel and the second channel allowing simultaneous independent access to the first memory device and the second memory device.

78. The bus system of claim 72 further comprising a third module coupled to first channel and the second channel via the motherboard connectors.

79. The bus system of claim 72 wherein the first module further includes a first IC coupled to the first channel, and the second module includes a second IC coupled to the second channel.

80. The bus system of claim 79 wherein the first module further includes a third IC coupled to the second channel and the second module further includes a fourth IC coupled to the first channel.

81. The bus system of claim 80, wherein the first, second, third and fourth ICs are memory devices.

82. The bus system of claim 80 further comprising a first request channel coupled to the first memory device and the third memory device and a second request channel coupled to the second memory device and the fourth memory device.

83. The bus system of claim 72 wherein the bus segments further couple additional ingress connectors and additional egress connectors on the first module and the second module to provide a third channel and a fourth channel.

84. The bus system of claim 83 wherein the first channel, the second channel, the third channel, and the fourth channel allow simultaneous independent access to a plurality of ICs including a first IC of the first module and a second IC of the second module.

85. A module having first and second primary surfaces and having a first end, the module comprising:

a first integrated circuit (IC) populating at least one of the first and second primary surfaces;

a first set of input finger connectors disposed on at least one of the first and second primary surfaces;

a first set of output finger connectors disposed on at least one of the first and second primary surfaces;

a second set of input finger connectors disposed on at least one of the first and second primary surfaces;

a terminator disposed on at least one of the first and second primary surfaces;

a first bus including a first channel extending from the first set of input finger connectors to the first set of output finger connectors, the first bus connected to the first IC; and

a second bus including a second channel extending from the second set of input finger connectors to the terminator.

86. The module of claim 85 further comprising:

a second IC, wherein the second bus is coupled to the second IC.

87. The module of claim 86 wherein the first channel and the second channel allow simultaneous independent access to the first IC and the second IC.

88. The module of claim 85 wherein the first set of input finger connectors and the second set of input finger connectors are disposed proximate to the first end.

89. The module of claim 85 further comprising:

a third integrated circuit (IC) populating at least one of the first and second primary surfaces;

a fourth integrated circuit (IC) populating at least one of the first and second primary surfaces;

a third set of input finger connectors disposed on at least one of the first and second primary surfaces;

a second set of output finger connectors disposed on at least one of the first and second primary surfaces;

a fourth set of input finger connectors disposed on at least one of the first and second primary surfaces;

a second terminator disposed on at least one of the first and second primary surfaces;

a third bus including a third channel extending from the third set of input finger connectors to the second set of output finger connectors, the third bus connected to the third IC; and

a fourth bus including a fourth channel extending from the fourth set of input finger connectors to the second terminator.

90. The module of claim 89 wherein the first channel, the second channel, the third channel, and the fourth channel allow simultaneous independent access to the first IC, the second IC, the third IC, and the fourth IC.

91. The module of claim 89 wherein the first set of input finger connectors, the second set of input finger connectors, the third set of input finger connectors, and the fourth set of input finger connectors are disposed proximate to the first end.

92. The module of claim 89 wherein the first set of input finger connectors and the second set of input finger connectors are disposed on the first primary surface, and the third set of input finger connectors and the fourth set of input finger connectors are disposed on the second

primary surface.

93. The module of claim 85 wherein the first channel has a first characteristic impedance and is coupled to a plurality of paths, and wherein the plurality of paths have a combined effective impedance substantially equal to the first characteristic impedance.

94. A module comprising:

a printed circuit board;

a first set of integrated circuits (ICs) mounted on the printed circuit board;

a second set of ICs mounted on the printed circuit board;

a first input connector disposed on the printed circuit board; and

a first ingress bus coupled to the first input connector, the first ingress bus split into a first path and a second path, the first path coupled to the first set of ICs and the second path coupled to the second set of ICs, the first ingress bus having a first characteristic impedance and the first path and the second path having a combined effective impedance substantially equal to the first characteristic impedance.

95. The module of claim 94 wherein the first path is coupled to a first terminator and the second path is coupled to a second terminator.

96. The module of claim 94 wherein the module further comprises:

a first output connector disposed on the printed circuit board; and

a first egress bus coupled to the first output connector, the first path and the second path merged into the first egress bus, the first egress bus having a second characteristic impedance substantially equal to the first characteristic impedance.